REMARKS

In the Office Action dated February 17, 2004, Examiner rejected claims 1-16. Regarding Claim 3, Examiner indicated that it would be allowable if rewritten in independent form. Claim 3 has not been rewritten in independent form in the current amendment because Claim 1 from which it depends is now believed to be allowable.

Examiner rejected claims 1, 2 and 4-16 under 35USC102(e) as being anticipated by Carlson US 6,167,526. A portion of the rejection stated that: "The early signals are ORed together and form a "scaled down" timing signal. The late signals ore ORed together to form a "scaled down" timing signal. These "scaled down" timing signals are input to the detection counter which outputs an adjust signal for adjusting the window signal (figure 3 and column 5, lines 7-28). The detection counter is an "integrator" in that it outputs the signal that modifies the window signal. The detection counter will generate an early and late count from the outputs of the OR gates and will increment the count or decrement the count accordingly." Claims 4-7 were further rejected on the basis that: "the counts are incremented when an early or late pulse is detected. Any component of the pulse that is detected will indicate an early or a late pulse (column 7, lines 12-15)." (It is believed that Examiner intended column 5, lines 12-15. In any case, these early or late pulses are not "scaled down" as explained herein.)

It is noted at the outset that the Carlson patent teaches a technique for synchronizing a decoder circuit with a phase-encoded data signal representing data stored in a disc drive. In an ideal signal, the data pulses would align exactly with the detection window centers (col. 1 lines 54-55). A self-clocking decode phase locked loop uses each pulse in the data signal to adjust the start of the window immediately following the pulse. (col 2 lines 14-16). As shown in FIG. 1 (PRIOR ART), these pulses are provided directly to the GENERATE DETECTION WINDOWS block. This has some disadvantages as noted in the patent. To overcome these disadvantages, Carlson provides the circuitry on the right side of FIG. 3. In particular, the output of OR circuits 352 and 353 are provided to Up/Down "detection counter" 370 (instead of directly to the

GENERATE DETECTION WINDOWS block in FIG. 1). The output of Up/Down Counter 370 is then further processed and provided to block 308. Thus, as noted at column 2 lines 61-66: "Rather than shifting the detection windows on every occurrence of an early or late pulse within a detection window, the present invention counts the number of early and late pulses, and applies one or more thresholds to intelligently adjust the timing of the detection windows." (emphasis added) It appears that Examiner has analogized this feature with Applicant's scaling down of input signals to the integrator. However, the count up and count down inputs to UP/Down Counter 370 are the same signals that were previously applied to block 308. Therefore, these inputs to UP/Down Counter 370 are not "scaled down".

In contradistinction to the teachings of Carlson, Applicant addressed the problem of high frequency limitations associated with integrators (which Examiner has analogized with Up/Down Counter 370). The problem recognized and solved by Applicant is described in the instant application at page 3 line 30 to page 4 line 5. As there noted, high frequency integrator operation typically results in high power consumption, heat dissipation problems, and the design of complex, and accordingly expensive, integrators that are able to perform high frequency integration. There is no teaching anywhere in Carlson that this problem was either understood or resolved.

In order to reduce the frequency of input signals to integrator 512 (see FIG. 5), Applicant provides a pulse accumulator 550, which is configured to divide by some discrete integer number such as 4 or 16, for example. (See page 14 line 28 to page 15 line 2 in the instant application). As there noted, other divisors may be used to scale down the early/late counts before they are provided to the integrator. Such a division and scaled down count is not taught or contemplated by Carlson. The term "scaled down" as used by Examiner in the rejection of the claims is language borrowed from the instant application. The structure and function taught by Carlson, in fact, does not anticipate Applicant's structure or function and most certainly does not achieve the desired result of reducing the frequency of operation of the integrator.

For the foregoing reasons, and as further noted hereinbelow, Applicant respectfully traverses the rejection of claim1, which recites:

> An early-late pulse accumulator comprising:
>
> a first logic device configured to toggle a first output logic level upon receipt of an early pulse;
>
> a second logic device configured to toggle a second output logic level upon receipt of a late pulse, wherein the first and second logic devices are configured to allow only one of the first and second output logic levels to be toggled at a time;
>
> a first ripple divider configured to receive the first output logic level and to provide a scaled down count of the number of times the first logic device toggles;
>
> a second ripple divider configured to receive the second output logic level and to provide a scaled down count of the number of times the second logic device toggles;
>
> a first synchronizing logic device configured to receive the scaled down count of the number of times the ~~second~~ first logic device toggles and to generate a first terminal count signal proportional to the number of early pulses received by the first logic device;
>
> a second synchronizing logic device configured to receive the scaled down count of the number of times the second logic device toggles and to generate a second terminal count signal proportional to the number of late pulses received by the second logic device; and
>
> an integrator configured to receive the first and second terminal count signals and generate a net early-late count.

Note at the outset, that Carlson does not teach a pulse accumulator, as recited in the preamble. Nowhere in Carlson is there a teaching of first and second logic devices to provide a toggle function. Nowhere in Carlson is there a teaching of first and second ripple dividers as discussed for example at page 16 line 30 to page 17 line 4. Nowhere in Carlson is there a teaching of first and second synchronizing logic devices configured to receive scaled down counts. Lastly, although Applicant's integrator has been analogized with Carlson's Up/Down Detection Counter 370, it does not receive a reduced frequency, i.e. scaled down, input. In view of the foregoing, it is

respectfully urged that Claim 1 is allowable. It has been amended herein merely to correct a clerical informality.

Dependent claims 2, 3, 4, 5, 6, and 7 are believed to be allowable for the same reasons and that they recite additional features of the invention. By way of example, claim 3 was indicated as being allowable by expanding on the structural details of the first and second logic devices that perform the toggle functions. It is respectfully noted that since Carlson does not teach or suggest the toggle functions as claimed in Claim 1 in connection with the first and second logic devices, Claim 1 is allowable even without the added limitation of Claim 3.

Claim 8 was rejected under the same rationale as claim 1. The rejection of claim 8 is respectfully traversed and claim 8 is believed to be allowable for the same reasons as Claim 1. In addition, claim 8 has been amended to more succinctly set forth Applicant's invention. Amended Claim 8 recites:

A pulse accumulator comprising:

a logic device for receiving more than one early pulse and more than one late pulse;

an early ripple divider configured to count the early pulses on a scaled down basis;

a late ripple divider configured to count the late pulses on a scaled down basis;

an early pulse synchronizing device configured to receive the scaled down early pulses and to generate an early terminal count corresponding to the number of early pulses;

a late pulse synchronizing device configured to receive the scaled down late pulses and to generate a late terminal count corresponding to the number of late pulses;

an integrator configured to receive a scaled down clock signal and to increment upon receipt of the early terminal count signals and decrement upon receipt of the late terminal count signals.

With reference for example to Applicant's Figs. 6, 9, 10, 13, and 14, note that the integrator receives a scaled down clock signal. Although the Up/Down Detection Counter 370 in FIG. 3 of Carlson receives many inputs, none of them are a scaled down clock signal. In fact, Carlson's invention is in the field of self-clocking decode phase locked loops (col. 2 lines 59-80). Self-clocking implies no unique clocking function. This is further proof that utilization of the early/late signals to count up and down in block 370 and perform the late and early adjustments of the windows in device 308 is unrelated to Applicant's invention of operating a digital integrator at a reduced frequency.

Independent claim 9 was rejected on the basis that: "Carlson discloses a method for synchronizing an output signal to a data signal. Carlson discloses this method in figure 3. A data signal is received in elements 324 and 326. The data signal is compared to a window signal that is adjusted by the output signal (figure 3 and column, lines 25-46. A timing signal is generated by these elements indicating the phase relationship between the data signal and the window signal. These signals are output to the OR gates 352 and 353. The signals are ORed together and form "scaled down" timing signals. These "scaled down" timing signals are input to the detection counter which outputs an adjust signal for adjusting the window signal (figure 3 and column 5, lines 7-28). The detection counter is an "integrator" in that it outputs the signal that modifies the window signal." (emphasis added)

Applicant disagrees with Examiner's characterization of "scaled down" timing signals being input to the detection counter. As previously noted, the output of OR gates 352 and 353 appear to be identical to the outputs of the corresponding OR gates in FIG. 1 (PRIOR ART) and are not "scaled down". Therefore the timing signals that are input to the detection counter are not scaled down. Claim 9 claims the invention, as follows:

> A method for synchronizing an output signal to a data signal, the method comprising the steps of:
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> receiving a data signal at a phase detector;
>
> receiving an output signal at the phase detector;

comparing the data signal and the output signal in the phase detector;

generating, in the phase detector, a timing signal indicating the relative phase relationship between the data signal and the output signal;

dividing the timing signal to generate a scaled down timing signal;

receiving the scaled down timing signal at an integrator; and

generating in the integrator a control signal for modifying the output signal to synchronize the output signal to the data signal.

In addition to the previously noted distinctions, note that nowhere in Carlson is there a suggestion to perform the method step of: dividing the timing signal to generate a scaled down timing signal. The absence of a teaching of this key method step by Carlson not only renders Carlson inoperative as a reference anticipatory to Claim 9 but also highlights the significance of this step in the overall combination of Applicant's invention. A rejection based on a reference that fails at the point of novelty should not be sustained. Claims 10 and 11, which depend from claim 9 should be allowable for the same reasons and also as they recite additional features of the invention.

Claims 12 and 16 were rejected by Examiner on the grounds that Carlson discloses a system for synchronizing an output signal to a data signal in figure 3. The portion of Examiner's rejection with which Applicant respectfully disagrees is the contention that: "The early signals are ORed together and form a "scaled down" timing signal. The late signals are ORed together and form a second "scaled down" timing signal. These "scaled down" riming signals are input to the detection counter which outputs an adjust signal for adjusting the window signal (figure 3 and column 5, lines 7-28). The detection counter is an "integrator" in that it outputs the signal that modifies the window signal." As previously noted, Carlson does not refer to the signals applied to the detection counter as "scaled down". In fact, there is no teaching in figure 3, at column 5, lines 7-28 or anywhere else in the Carlson patent that the inputs to the detection counter are "scaled down". This is because they are not "scaled down" and there is no suggestion or teaching for dividing the signals by any number or performing a "scaling down" function. Sending signals through OR gates as was done in the FIG. 1

(PRIOR ART) drawing is not "scaling down" (a term used and defined by the Applicant in the instant application). For these reasons, it is requested that the rejection of Claims 12 and 16 be withdrawn. The rejection of dependent claims 13-15 is also requested to be withdrawn for the same reasons and that they recite additional features. For example, claims 13-15 were rejected because Carlson's detection counter outputs an adjustment signal that adjusts the window signal. However, Carlson does not teach a phase selector configured to select a signal phase form among more than one signal phases provided by a voltage controlled oscillator, wherein the phase selector is configured to vary the frequency of the recovered clock as recited in Claim 13. Similarly, the details set forth in claims 14 and 15 are not found in Carlson.

In view of the foregoing, it is believed that claims 1-16, i.e. all the claims currently in this application are in condition for allowance. If Examiner has a question or comment or if Applicants' attorney can assist in any manner whatsoever, Examiner is respectfully requested to telephone the undersigned. An early notification of allowance is earnestly solicited.

Respectfully submitted,
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